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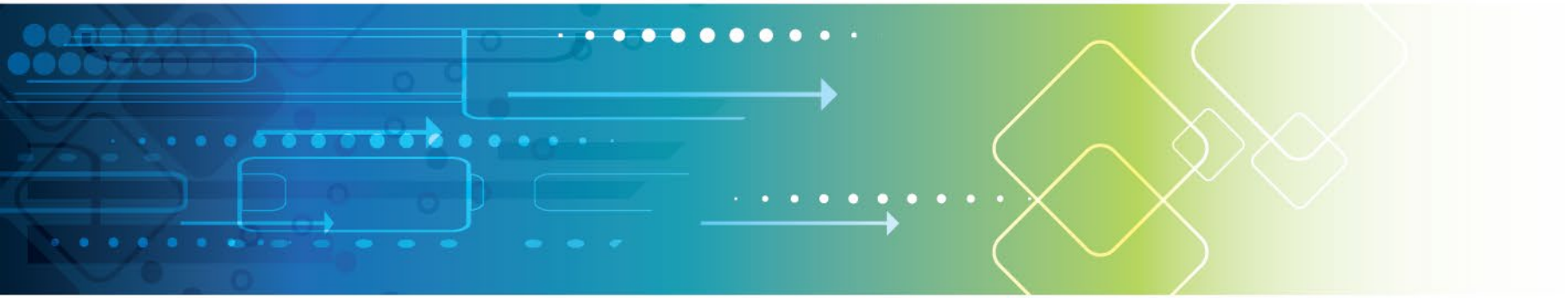
Emerging PMIC Trends Demand Test Innovations

Lauren Getz



Abstract

Power management integrated circuits (PMICs) are responsible for managing the power requirements for mobile systems while preserving the battery charge. New innovations in mobile PMIC devices such as integrating chargers makes a single device responsible for handling a plethora of requirements such as different charging schemes, modes and inputs, including wall, USB, and wireless. This component has become increasingly complex and embeds not only low drop out regulators, multi-phase DC-DC converters, USB fast chargers, general purpose analog to digital converters and communication interfaces but also other optional blocks such as LEDs, drivers, fuel gauges, and audio analog to digital / digital to analog converters. Testing high-performance PMICs requires high-density DC instruments with highly flexible merging capabilities to achieve high current.

This presentation will discuss the trends and requirements driving PMIC innovation and test solutions that maximize yield for high quality chips at the lowest cost of test.

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The Unsatiated Consumer- what do they want?

Features

Speed

Portability

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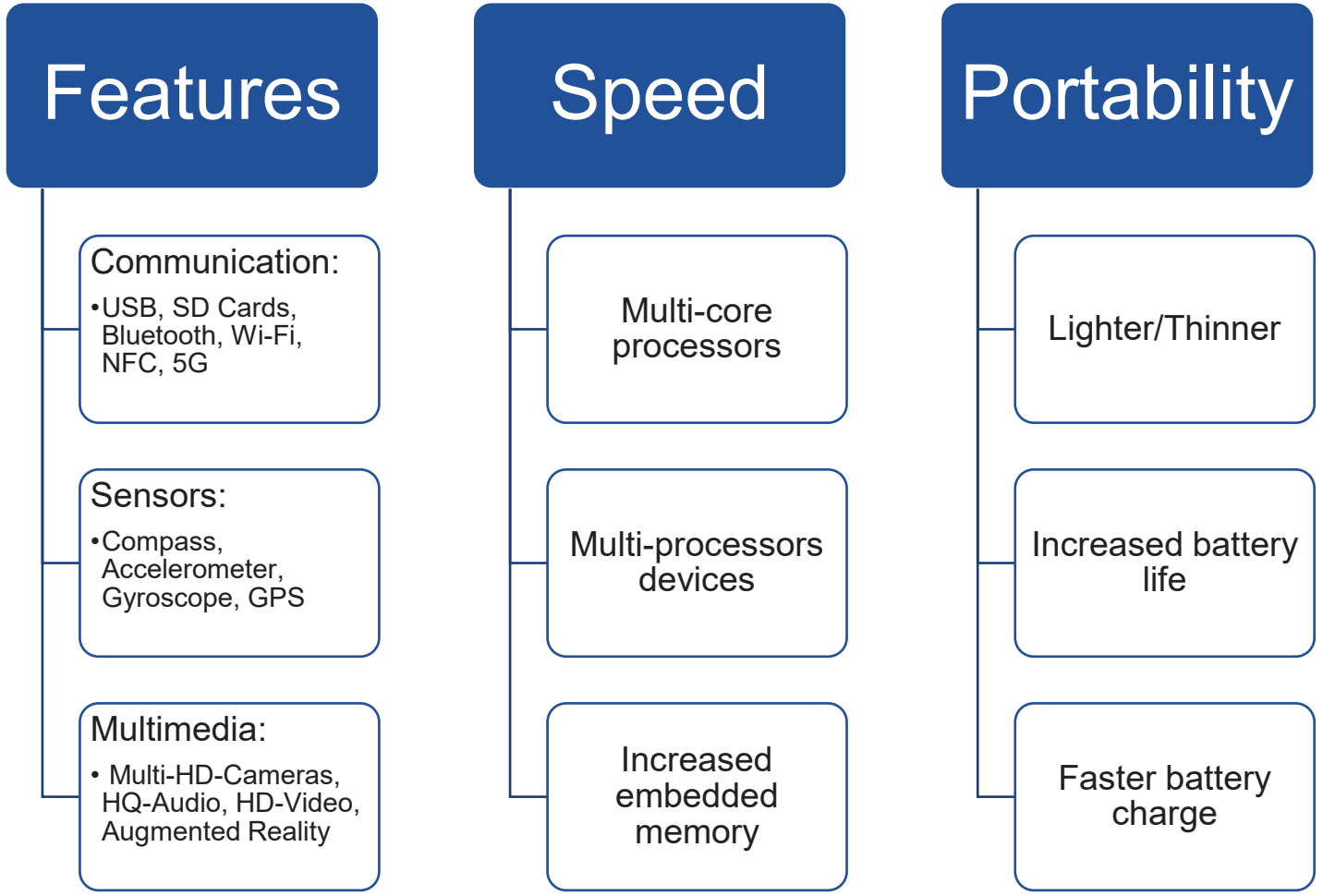
Translating Consumer Requests to Technical Improvements



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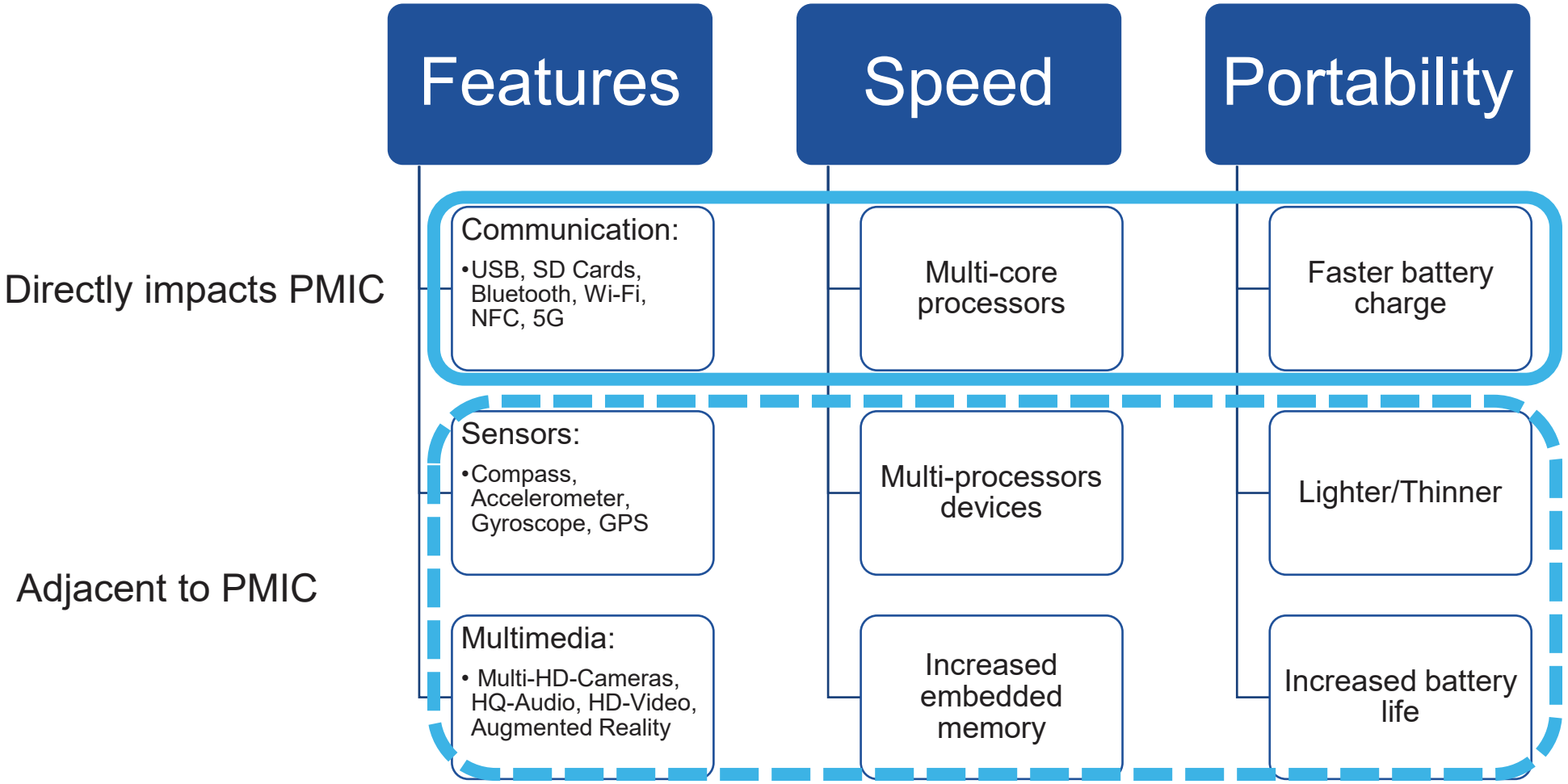
Translating Consumer Requests to Technical Improvements



Power requirements target both battery and Power Management IC improvements

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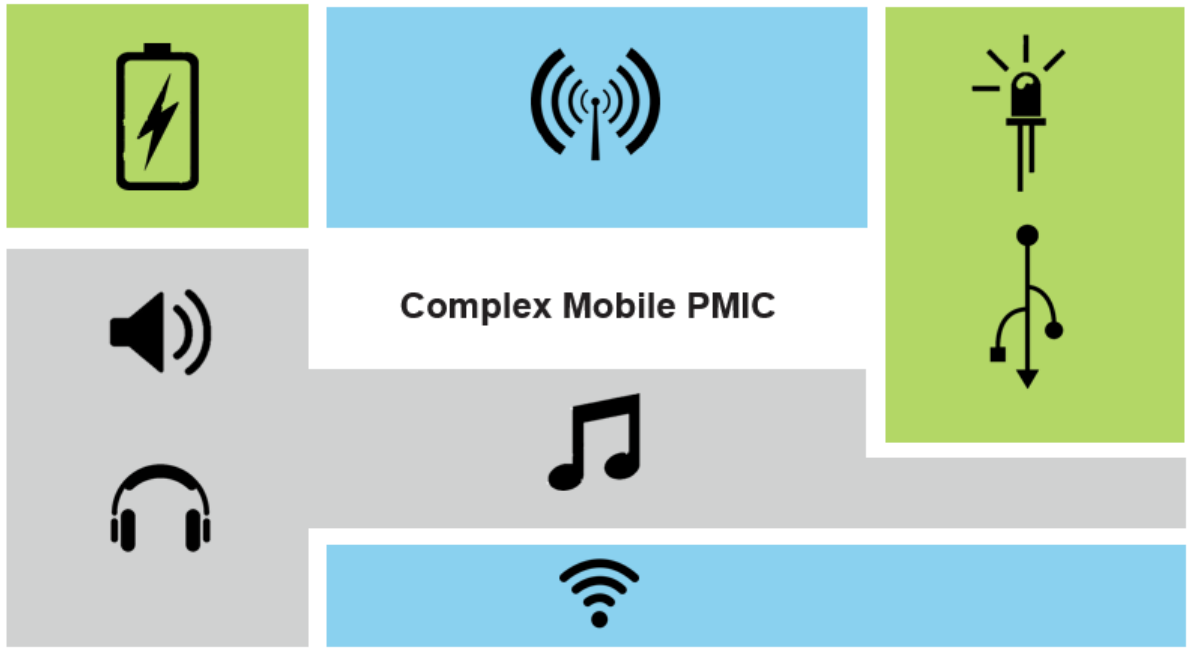
How is power managed?

The Power Management Integrated Circuit (PMIC) manages the power used by all the application blocks as well as the battery charge. Its role is to supply power to all the application's circuits while preserving battery charge by:

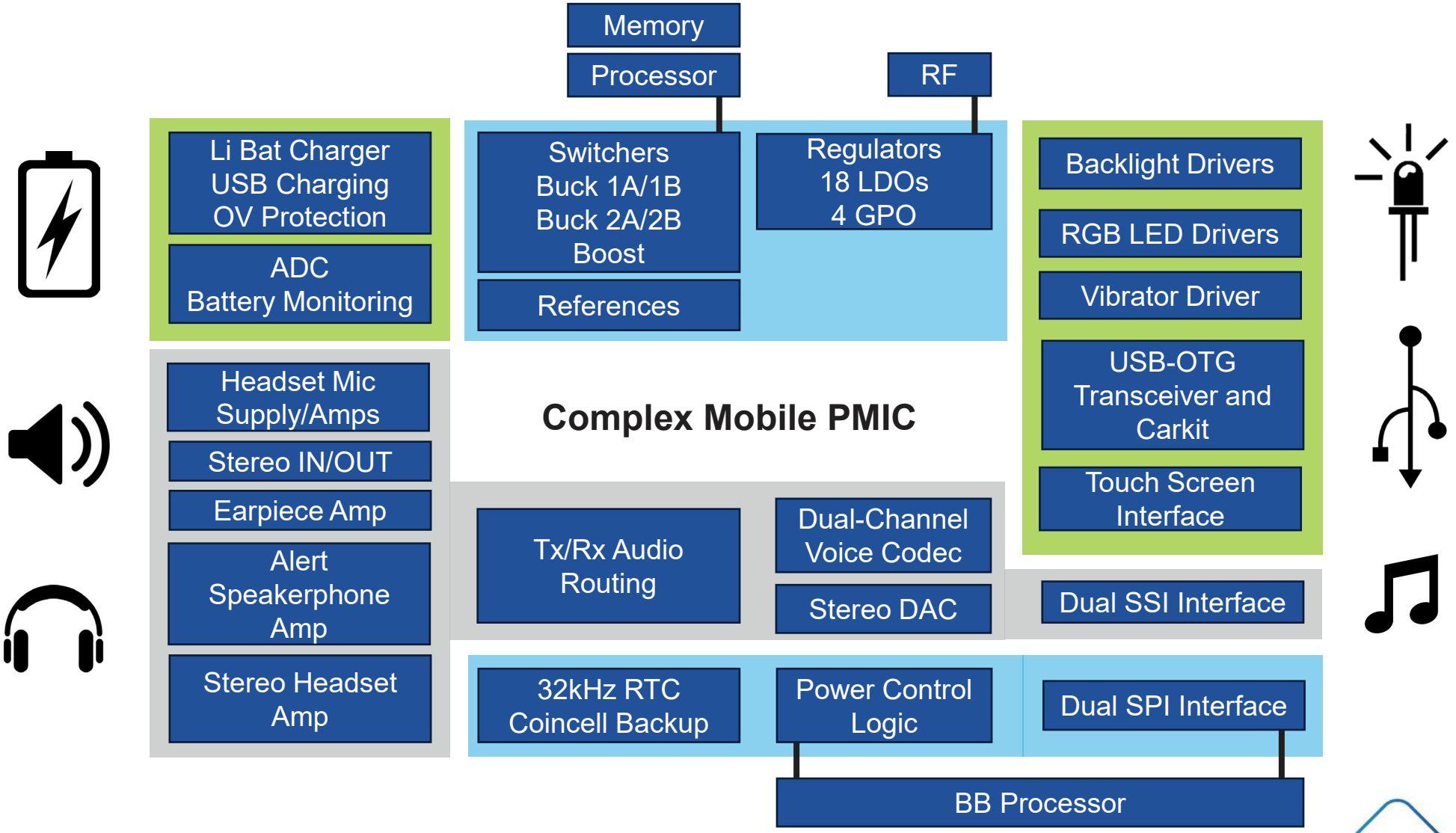
- Powering off unused functions
- Coordinating wake-up sequences to control current surges
- Scaling voltage dynamically
- Managing charge of battery from wall and USB supplies

High-end PMICs also embed:

- Drivers (Vibra, Keyboard and Backlight LEDs)
- Audio AD/DA converters, Amplifiers, Mux
- Video Interfaces (HDMI)
- Communication interfaces (USB-C, Ethernet, NFC)



Typical Complex Mobile PMIC



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Testing a Typical Complex Mobile PMIC

PMIC Device Blocks

- Low Integration: Voltage References, Linear Regulators (LDO), Switching Regulators (SMPS)
- High Integration: all above + Drivers, Audio, Video, USB-C, USB & Wall Charger

Pin count

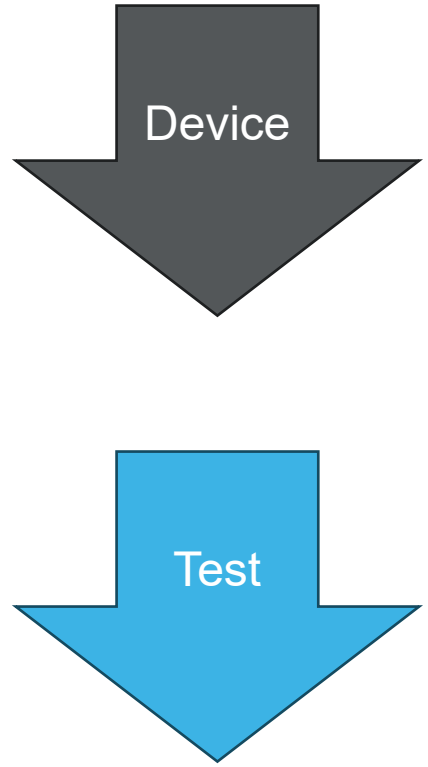
- Mid to high (up to 350pins)

Number of test sites

- Typical x16 sites today, moving up to x32 Sites

Typical Test Times and Parallel Test Efficiency

- Between ~3s and ~30s Single Site Test Time (depending on device complexity and level of DFT)
- Between ~95% and ~98% PTE (impacted mainly by device trimming)



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PMIC Trends
Where is the market going?
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Mobile PMIC Trends and Their Test Challenges

- Decreasing bandgap voltage with tighter trimming accuracy
- Embedded self trimming references
- Increasing SMPS output current and number of phases
- Increasing charger power with 240W Fast USB-C Chargers

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Decreasing bandgap voltage with tighter trimming accuracy

Why?

- One case is to increase the accuracy of the gas gauge
- Voltage sensed by the gas gauge must be a better ratio of the referenced voltage used by its converter

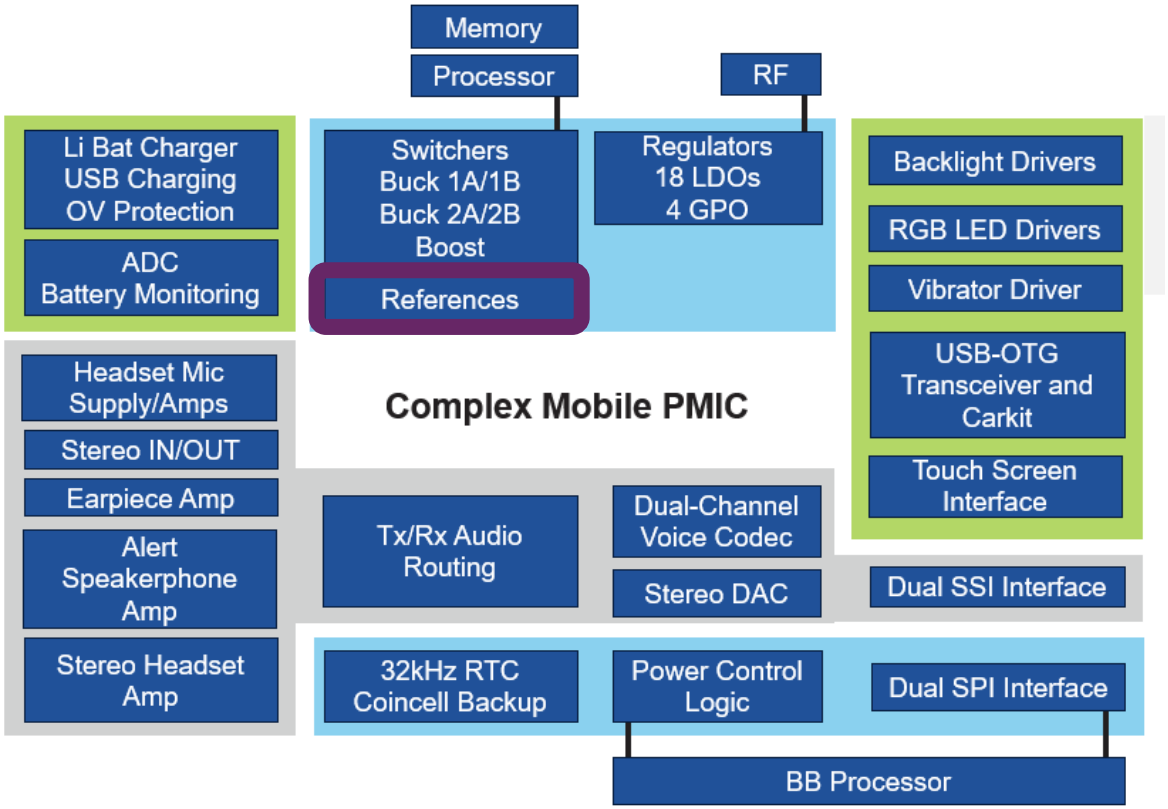
What does it mean for the PMIC?

- Decreasing Bandgap voltage from 1.2V->.9V->.75V
- Decreasing trimming steps down to 500uV

What does it mean for the tester?

- Needs better voltage measurement accuracy (at least 5 times better than the trimming step …)

Block	Test Requirements
Bandgap reference	100uV accuracy on <1.2V measurements



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Typical Test: Bandgap Voltage Adjustment

Test Description & Constraints

- Voltage references need to be trimmed very tightly to their target value to maximize the performances of the device
- The adjustment step is going down to 500uV
- These references are usually not buffered to avoid introducing offset error

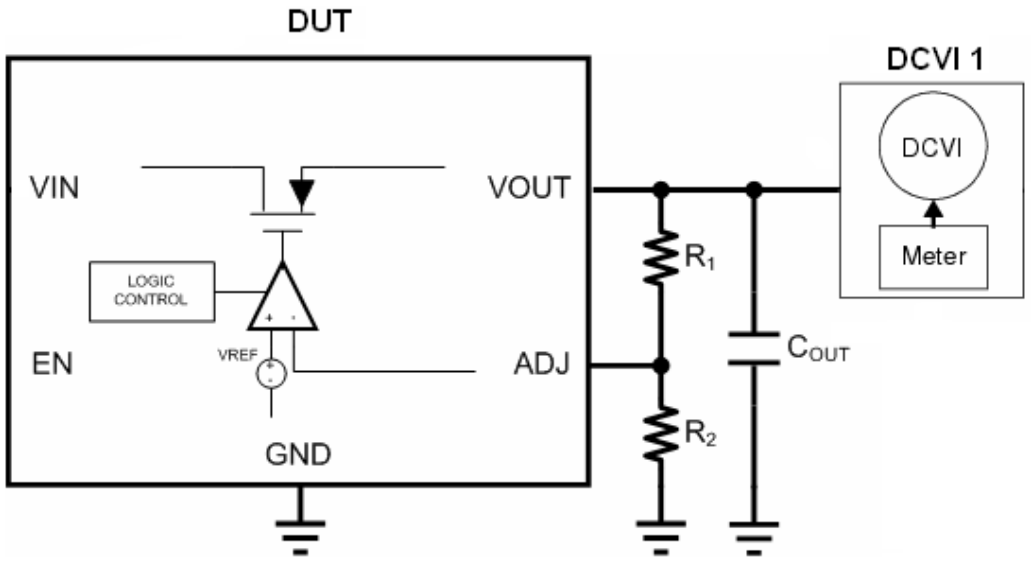
Instrument Requirements

- Being able to make voltage measurements with a maximum error of +/-100uV in a production environment without reducing the system utilization
- Provide a real high impedance, low leakage voltmeter connection

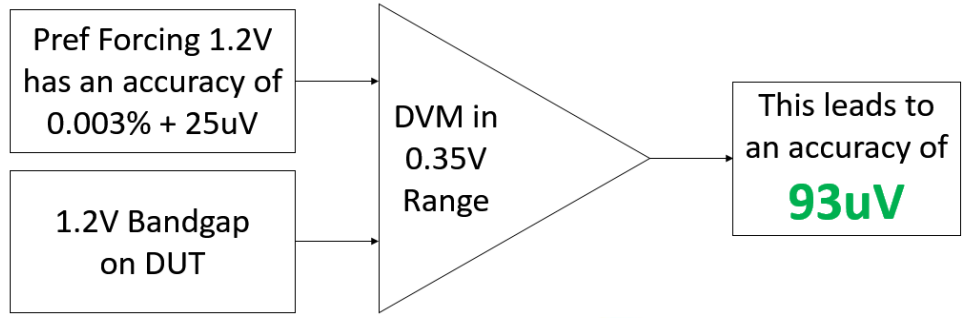
Solution

- 24 Bits ADC
- Voltage measurement accuracy ±(0.01% + 20uV + 10uV/V) in the 0.35V range with integrated gain/offset spot cal
- Input bias current <3nA on dedicated inputs
- Input impedance >100MOhms

Trim bandgap references with <100uV precision !



DVM in 0.35V Range and Spot Cal has an accuracy of 0.01% + 20uV + 10uV/V



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Embedded self trimming references

Why?

- Decreasing the time it takes to trim various voltage/current references and regulators
- To be able to trim multiple devices and blocks concurrently

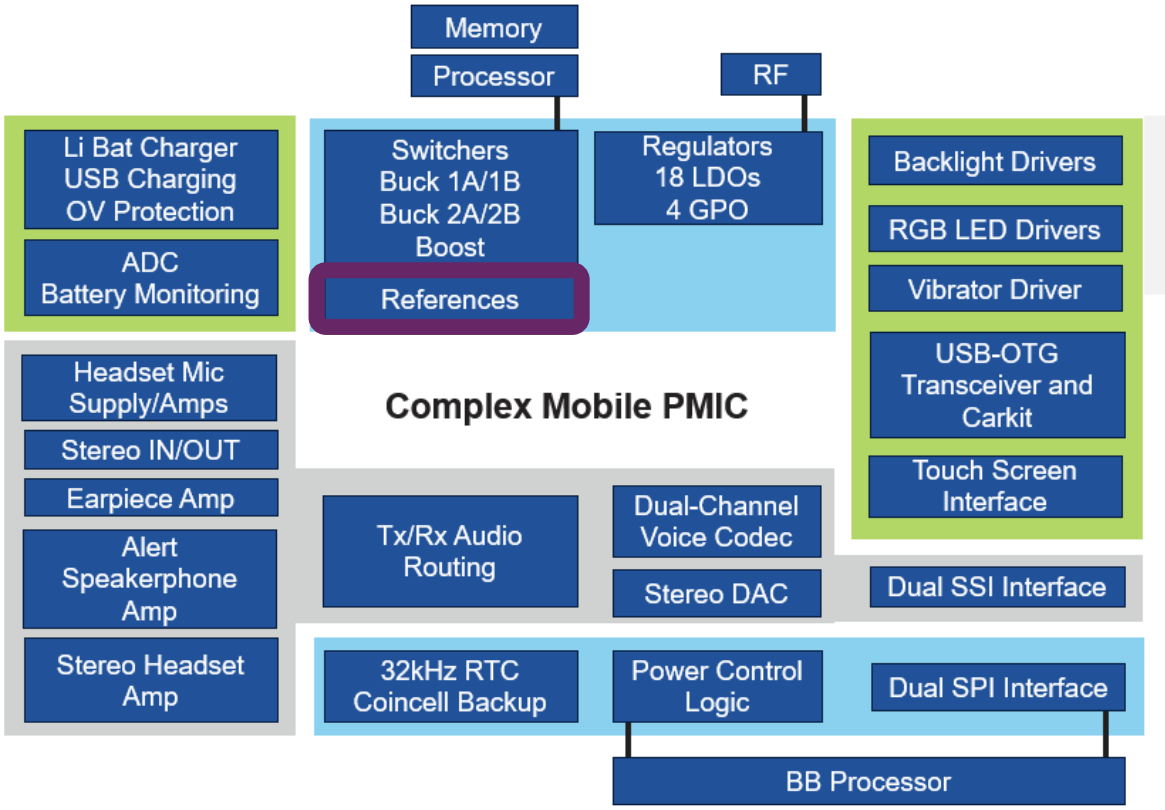
What does it mean for the PMIC?

- Needs to have some Design-For-Test with additional circuitry for self trimming

What does it mean for the tester?

- High accuracy requirements moved from the Meter to the Source
- Need to have very accurate programmable voltage/current sources

Block	Test Requirements
Bandgap Voltage Reference, Regulators	Precision Voltage Reference with 100uV accuracy at 1.2V
Current Reference	Precision Current Reference with few tens of nA accuracy



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Increasing SMPS output current

Why?

- Portable applications have to support more demanding blocks like Multicore Mobile Application Processors, GPUs

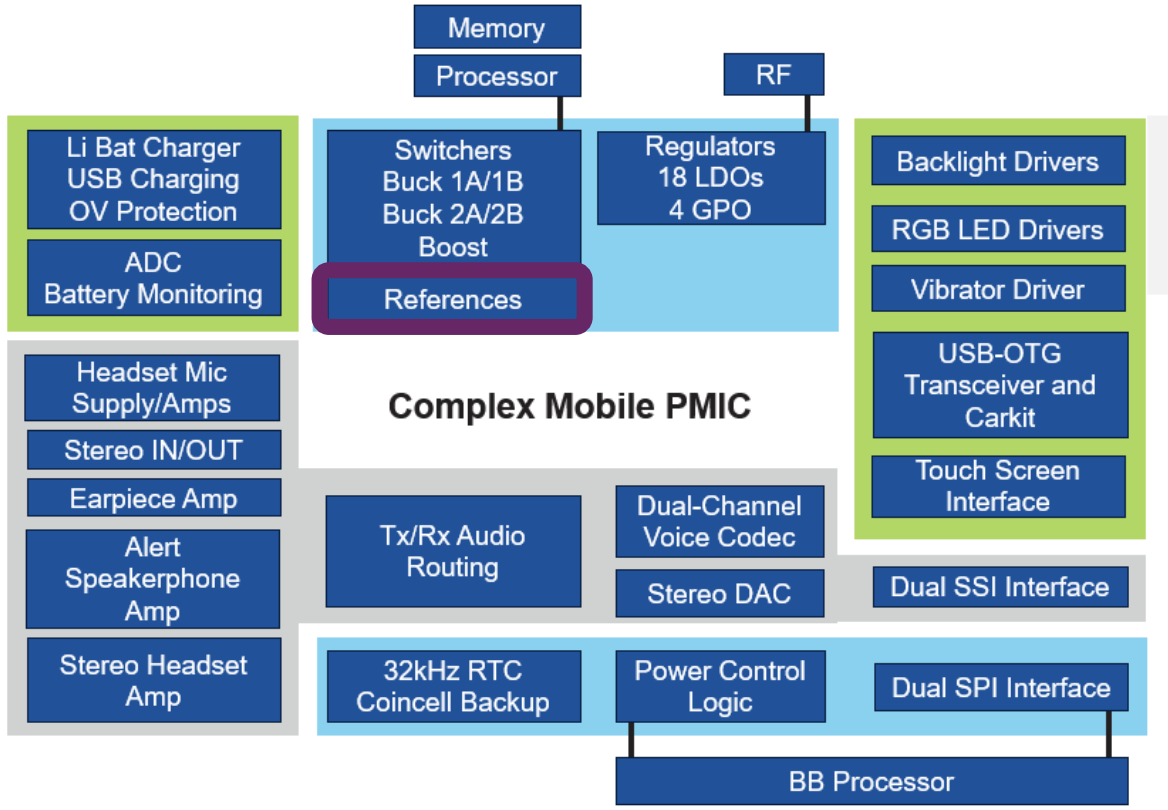
What does it mean for the PMIC?

- It has to provide and manage power for these blocks
- Up to 12 SMPS per die, capable of sourcing up to 10A each

What does it mean for the tester?

- Needs for high density DC instruments with high flexible merging capability to achieve high current

Regulator Type	Test Requirements
SMPS (up to 12 per die)	Voltage up to 6V Current up to 10A



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Typical Test: Current Limit aka OCP

Test Description & Constraints

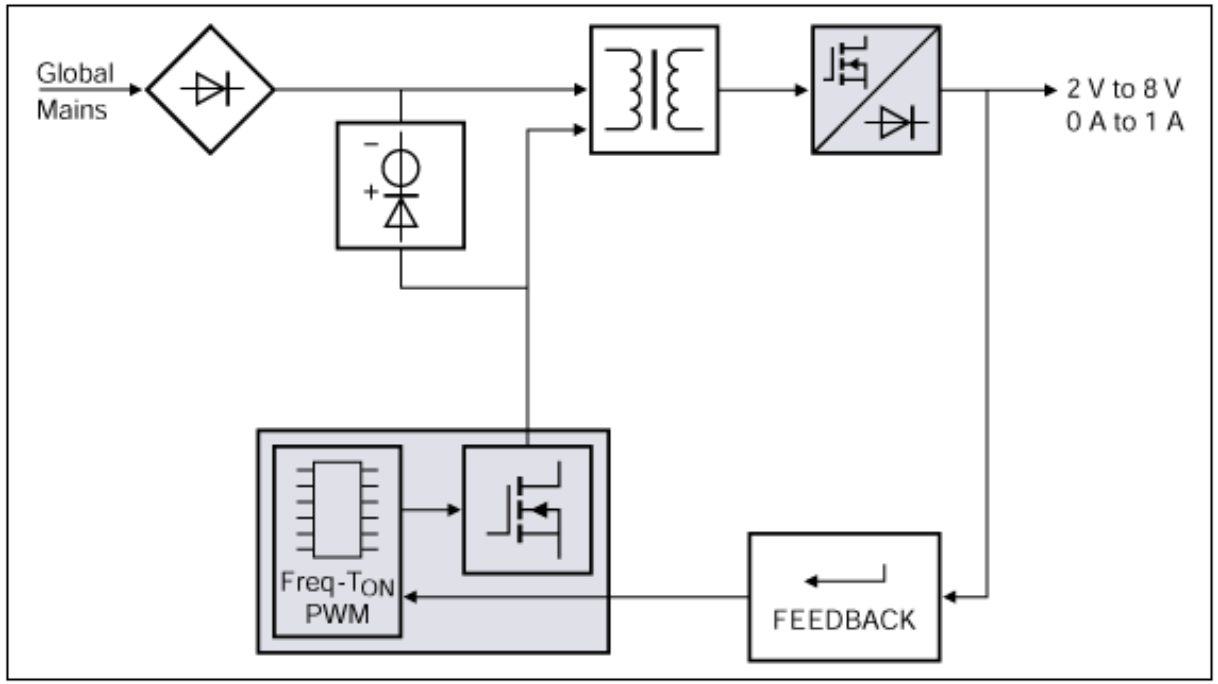
- Regulators need to be able to limit their current when their output are short-circuited to ground for protection issue
- This short circuit current can go up to 12A

Instrument Requirements

- Be able to force 0V and have up to 12A current flowing into it
- Be able to measure the current flowing
- Be able to run the test as fast as possible not to stress the device

Solution

- VI Channel on each regulator output pin
- Up to 2A current sink capability on every channels, mergeable up to 24A
- Current Measurement Accuracy ± (0.10% + 3mA + 300uA/V) in the 2A range
- Entirely controlled from pattern through PSets and uCodes



Test any regulator current limit up to 24A!

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Increasing number of SMPS phases

Why?

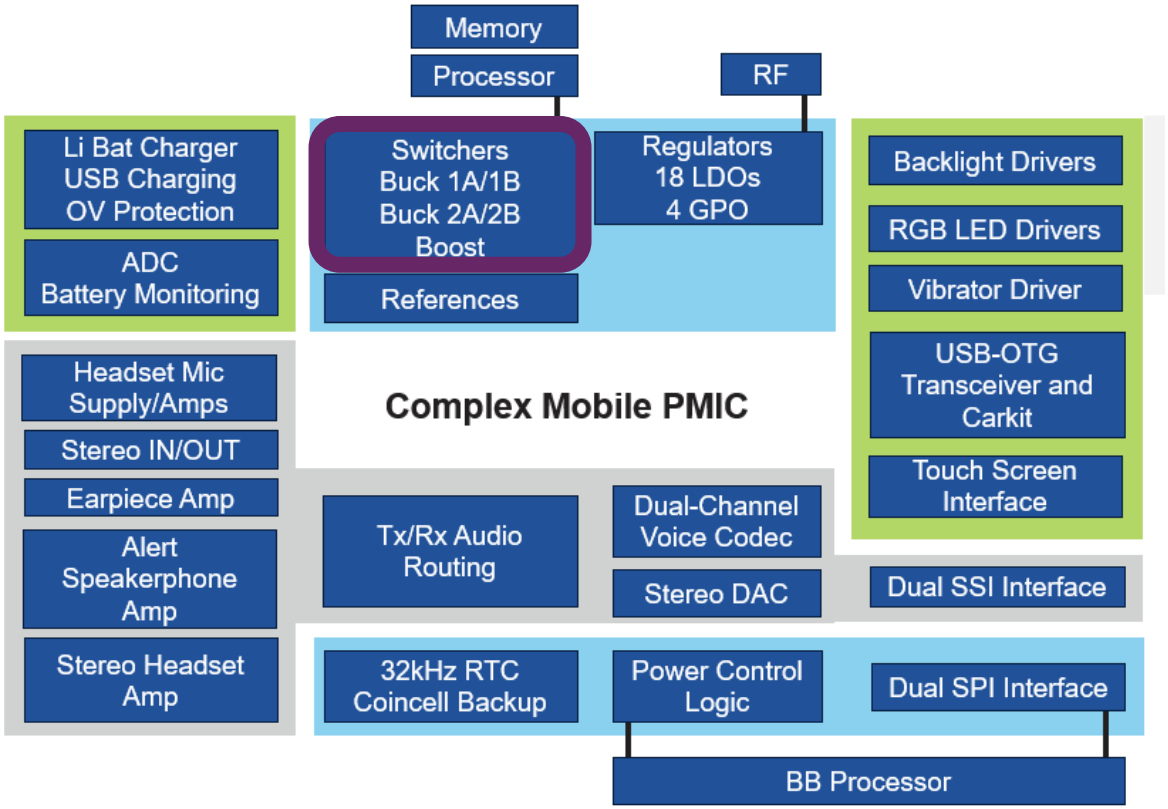
- Portable applications have to support more demanding blocks like multicore-processors
- Supporting higher current capability while preserving high power efficiency, a higher number of switching outputs need to be used

What does it mean for the PMIC?

- Each SMPS has more switching outputs
- Up to 5 output phases per SMPS

• What does it mean for the tester?

- Needs for high density DC instruments with high current capability and high accuracy
- Needs for integrated muxed outputs per channel to reduce the cost of the tester configuration as typically only 1 phase can be tested at a time in open-loop conditions, so a resource can be shared across all regulator's output phases



Regulator Type	Test Requirements
SMPS (up to 12 per die, up to 5 phases each)	Voltage up to 6V Current up to 2A per phase

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Typical Test: RDS On

Test Description & Constraints

- This test is performed by sourcing/sinking some known current (up to 2A) through the switching element of the SMPS and measuring the Voltage across it with a differential Voltmeter
- Typical limits are 100-200miliOhm. The desired Voltage measurement accuracy to support this measurement is <500uV on a common mode voltage of ~4V (Battery voltage).

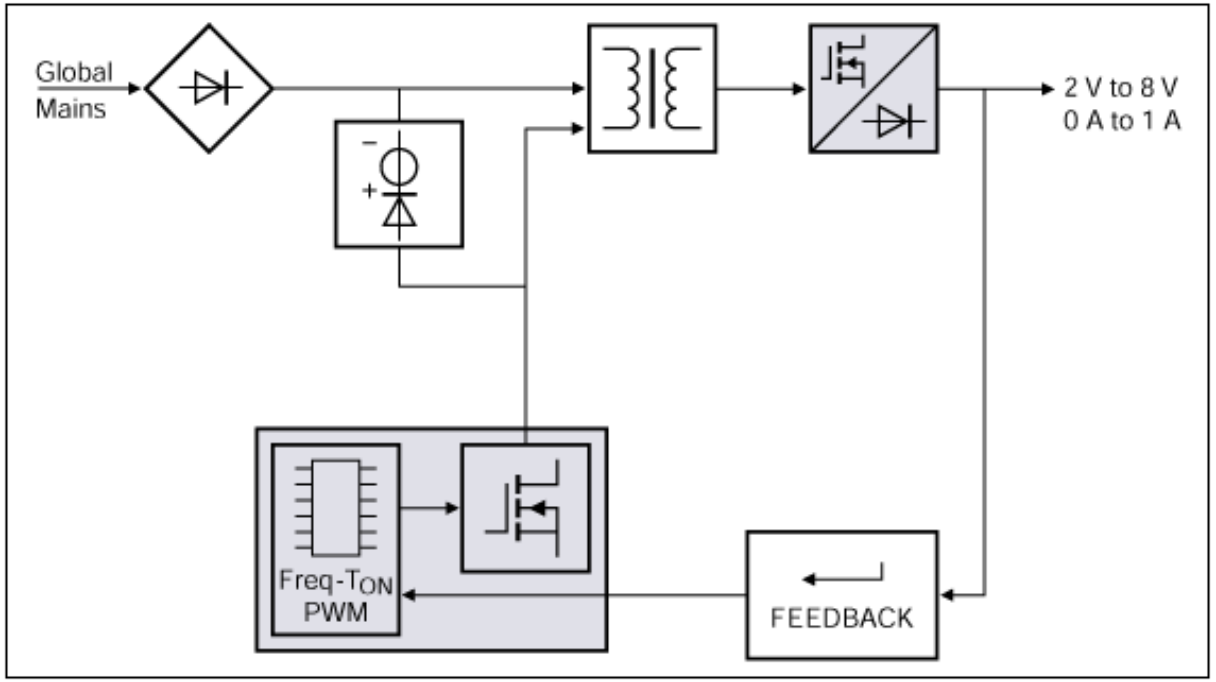
Instrument Requirements

- Source/sink an accurate current
- Measure an accurate differential voltage

Solution

- DC Instrument + High Precision Differential Meter
- VI Force Current Accuracy ± (0.20% + 3mA + 300uA/V) in the 2A range
- Differential Meter Accuracy ± (0.010% + 20uV + 10uV/V) with integrated spot cal

Make fast highly accurate RDSON measurements!



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Typical Test: Switching Frequency and Duty Cycle

Test Description & Constraints

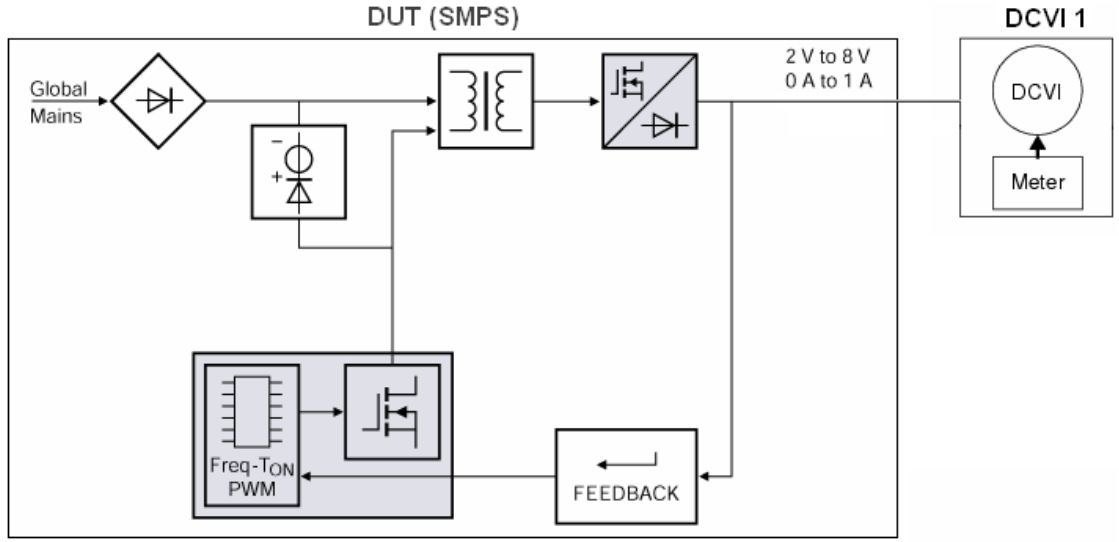
- Typical SMPS switching frequencies are ~2MHz, ranging up to 10MHz for high performance devices. Test limits for a typical 2MHz device are 1.95MHz – 2.05MHz, required accuracy for this test is <10kHz
- Typical max duty cycle measurements for SMPS devices are roughly 80-90%. For a 2MHz SMPS, that translates to a pulse-width measurement of ~425ns. Desired accuracy is ~10ns

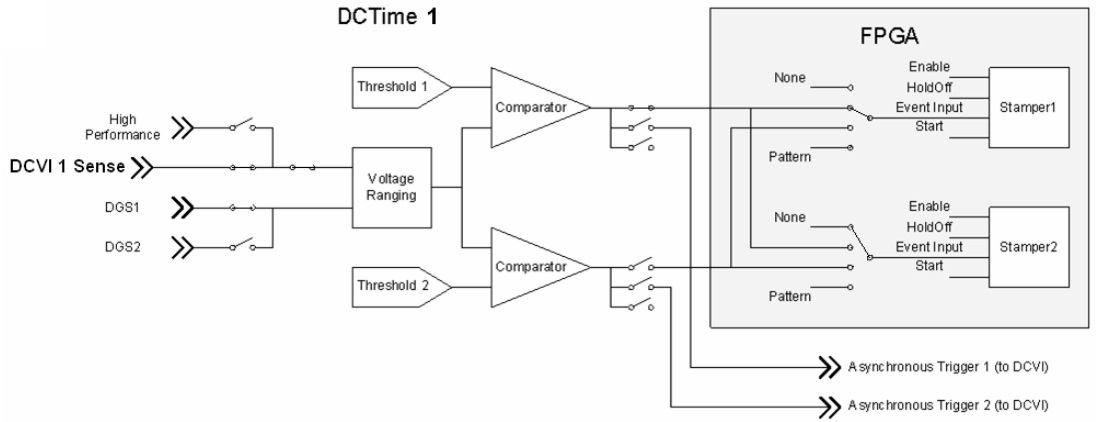
Instrument Requirements

- Be able to measure up to 10MHz signals with an accuracy of 10nS
- Have a wide enough voltage range

Solution

- VI Channel on the SMPS output pins
- Input Bandwidth up to 22MHz (up to 50MHz using the High-Performance Path)
- Input Voltage Range (-2.0V to 8.5V)
- Channel to channel skew 2nS
- Trigger Level Error ± (0.2% + 20.0mV)





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Increasing charger power with 240W Fast USB Chargers

Why?

- To support charge of batteries with increased power (Wearables->Phones->Tablets)
- To decrease the battery charge time (“superfast charge”)
- To standardize the charger across different devices and brands

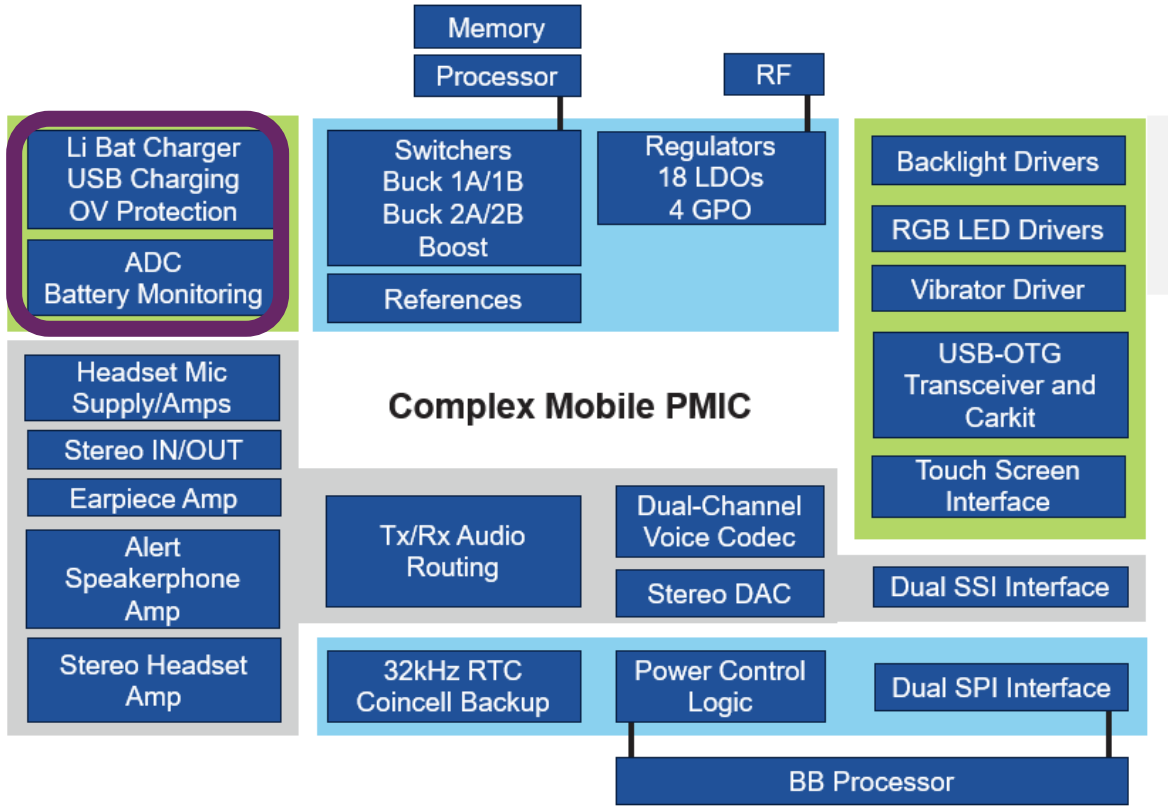
What does it mean for the PMIC?

- Fast 240W USB Chargers (USB-C, PD):
  - Input 48V@5A max and many other combinations of V/I within those limits
  - Output ~80W max up to ~8V
- DFT methods to support testing the charger at lower current not very common yet

What does it mean for the tester?

- Need DC instruments that can support various operating points at 240W power

Block	Test Requirements
USB Charger Input	48V max 5A max
USB Charger Output	6A @ 4.5V 10A @ 8V



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Typical Test: Power Efficiency

Test Description & Constraints

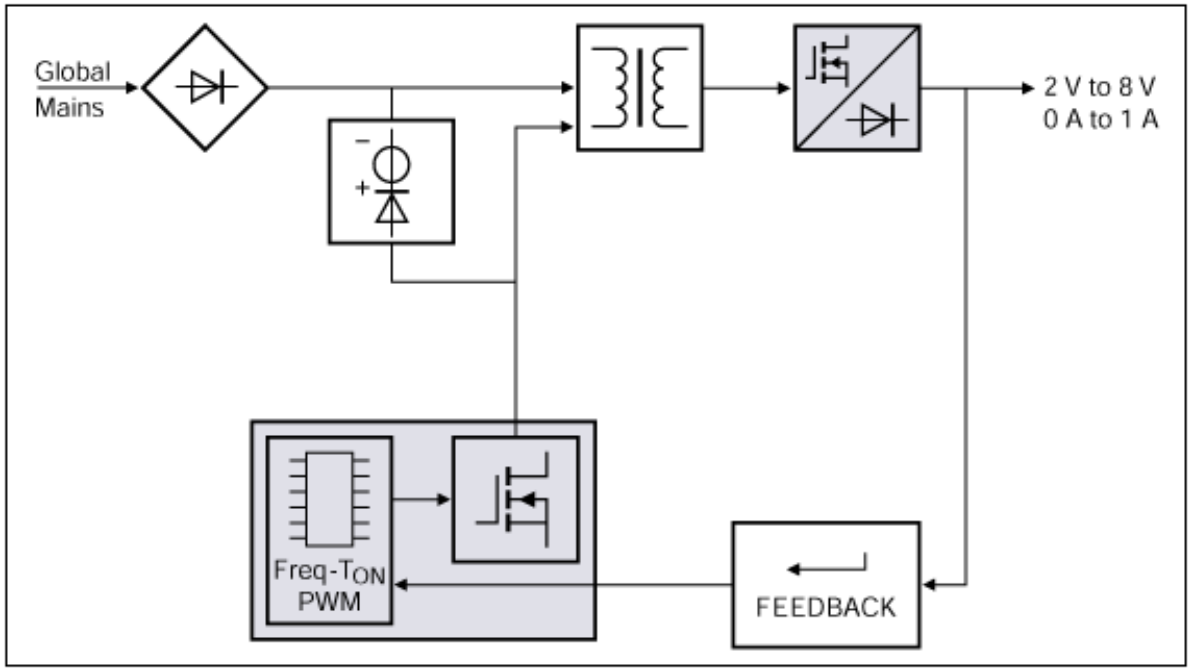
- This test is performed by forcing the nominal voltage on the charger input and sinking the max current on the charger output
- Input and output voltage and current are measured to compute the power consumed (input) and the power delivered (output)
- Power efficiency is calculated as the ratio of the delivered vs consumed power, expected efficiency is ~70% to 90%

Instrument Requirements

- Force an accurate voltage up to 20V voltage while delivering several Amps on input
- Sink up to 10A
- Measure voltage and current on both the input and output of the charger

Solution

- HVVI FV Accuracy ± (5.0mV + 0.05%), MI Accuracy ± (0.50% + 10mA)
- LVVI FI Accuracy ± (- 0.1% + 3mA), MV Accuracy ± (0.03% + 1.5mV)
- Flexible Merging up to 16A for HVVI and 24A for LVVI on an Integrated Mux



Test every 240W USB-C/PD Fast Chargers at any operating point!

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Building partnerships to solve the next generation of test!

Thank you

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