Elevating 3D NAND Performance

Dogwood and Its Process-Property Correlation for Low Resistivity, High Speed, and Superior Cell Performance

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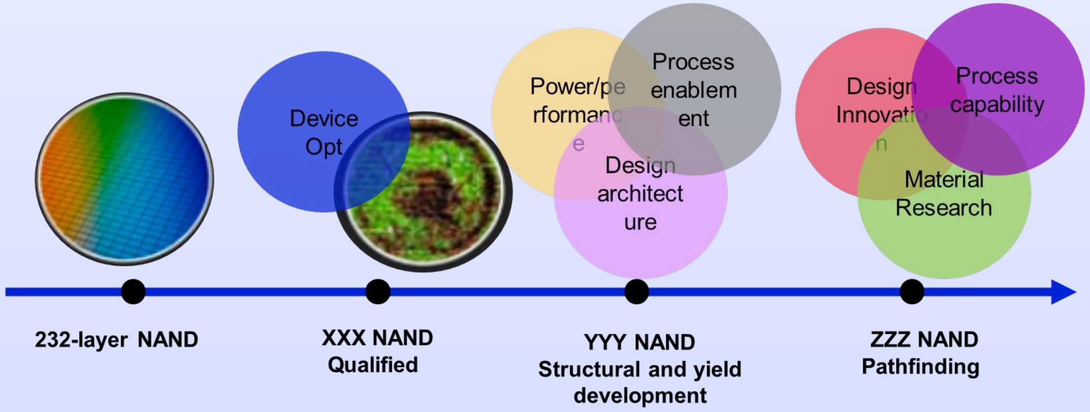
AGENDA

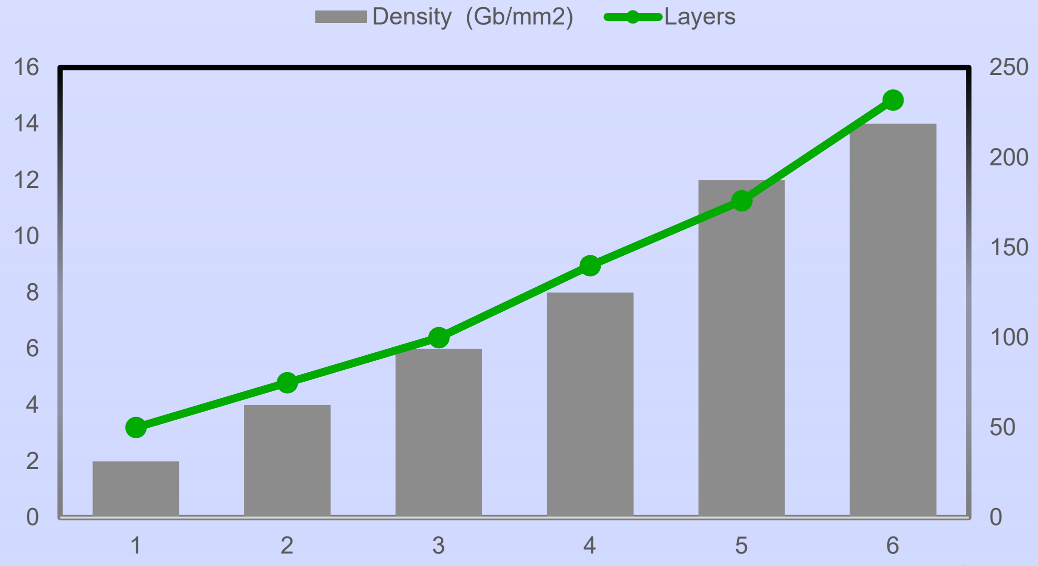
1. **Background -** Wordline Metal Evolution
2. **NAND Challenges -** Scaling and Metallization
3. **Introduction to Dogwood -** Brief history & exploration
4. **Summary and Conclusions**
5. Acknowledgements

3D NAND Tech | Innovations and Future trends

1. Micron pioneered transition from planar to 3D NAND
2. Vertical layer stacking to increase storage density
3. Higher capacity, lower power consumption and reduced cost per bit
4. Innovations such as QLC/PLC and CMOS under Array defines the future generations

Micron Roadmap for Leadership





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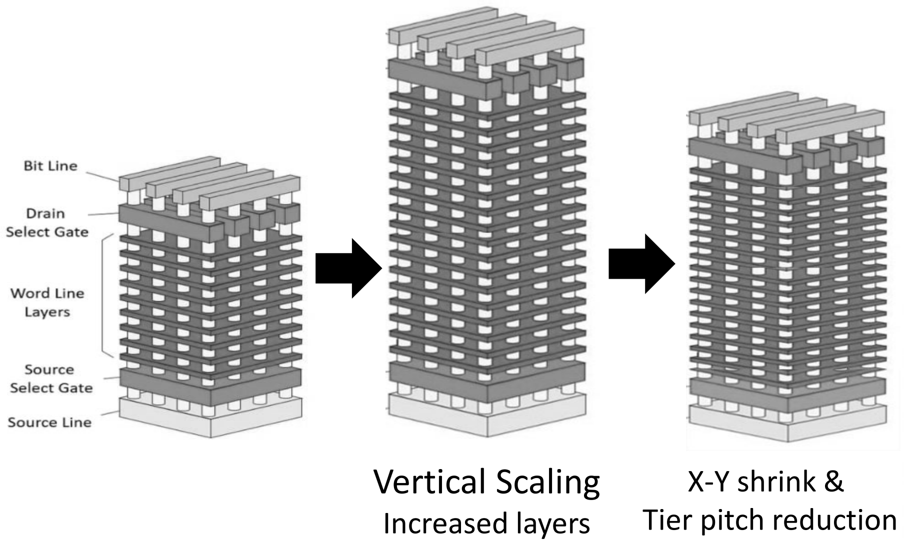
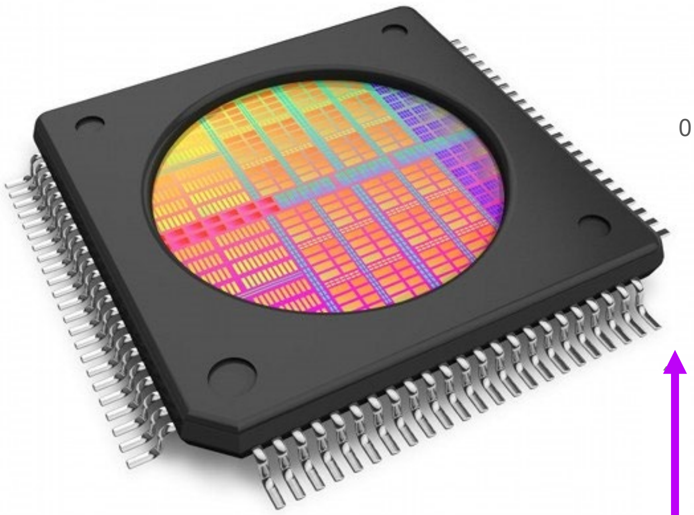
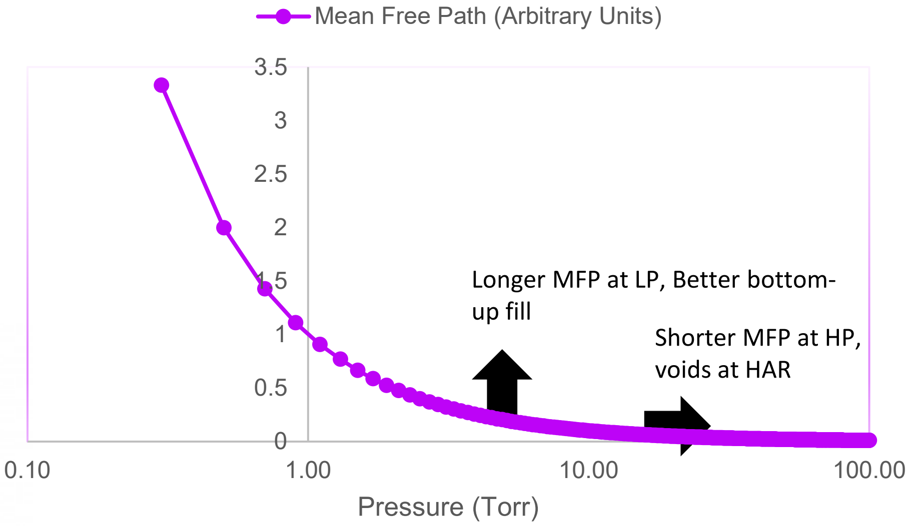
3D NAND Dev | Scaling & Metallization Challenges



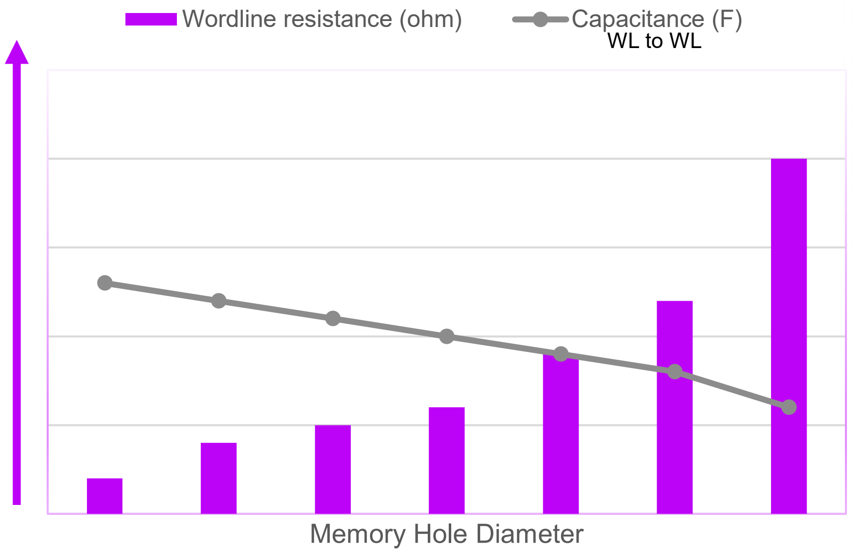
Vertical Scaling
Increased layers

X-Y shrink &
Tier pitch reduction

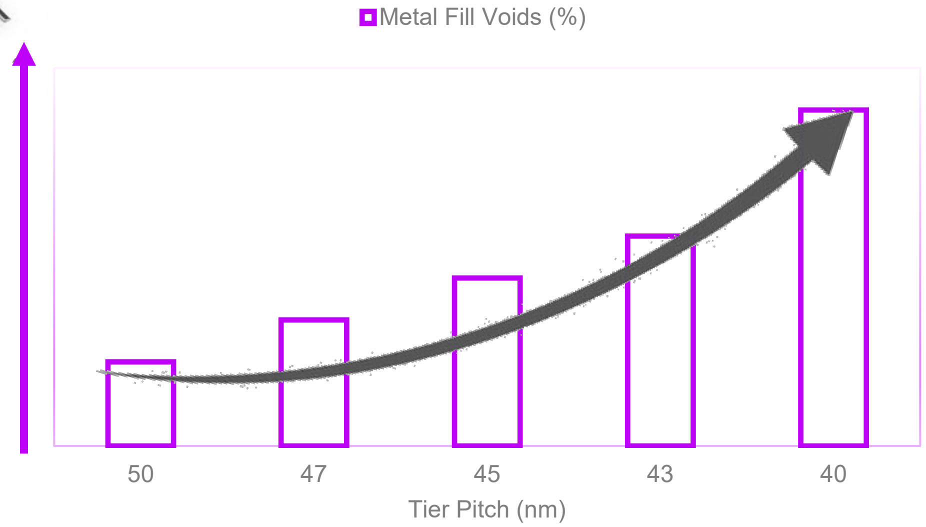




- As pressure increases, MFP decreasing, causing molecules to collide and lose its purpose



- Larger memory holes increase wordline resistance due to reduced cross-sectional area



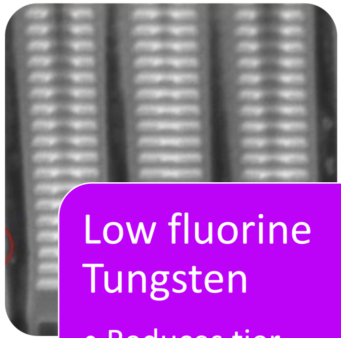
- X-Y shrink & Tier pitch reduction causes poor fill and increased wordline resistance

Seokkiu Lee ,2012, 4th IEEE International Memory Workshop, pp. 1–4.

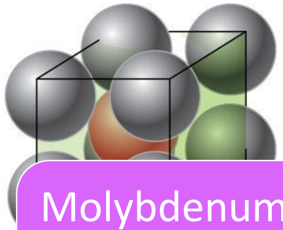
3D NAND | Wordline Metal evolution

Polysilicon Era
- High resistance
- Suitable for 2D NANDs

Tungsten
- Lower resistance
- Supports smaller tier pitch



Low fluorine Tungsten
- Reduces tier defects
- Improves reliability



Molybdenum
- Future scaling
- Lower resistance X Mean free path

Ruthenium (Next Gen)
- Excellent scalability and reduced RC delay

A. Ajaykumar *et al. 2021 Symposium on VLSI Technology*, Kyoto, Japan, 2021, pp. 1-2.

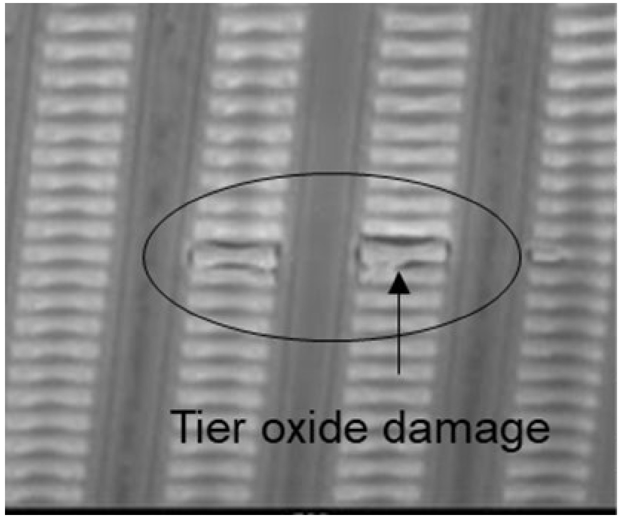
L. Breuil *et al.*,*IEEE International Memory Workshop (IMW)*, Dresden, Germany, 2020, pp. 1-4

Material selection Criterion for WL Metals

- Electrical Conductivity
- Thermal Stability
- Mechanical Strength
- Low electromigration Susceptibility
- Compatibility with dielectrics
- Cost effectiveness
- Scalability
- Chemical Stability

NAND PROCESS| Why Dogwood (DW)?

1 **F-free Precursor** ➡ No Tier oxide damage



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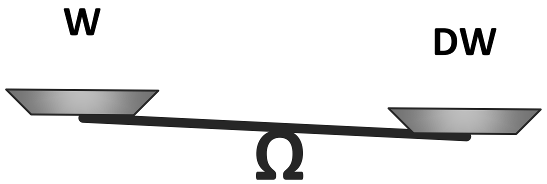


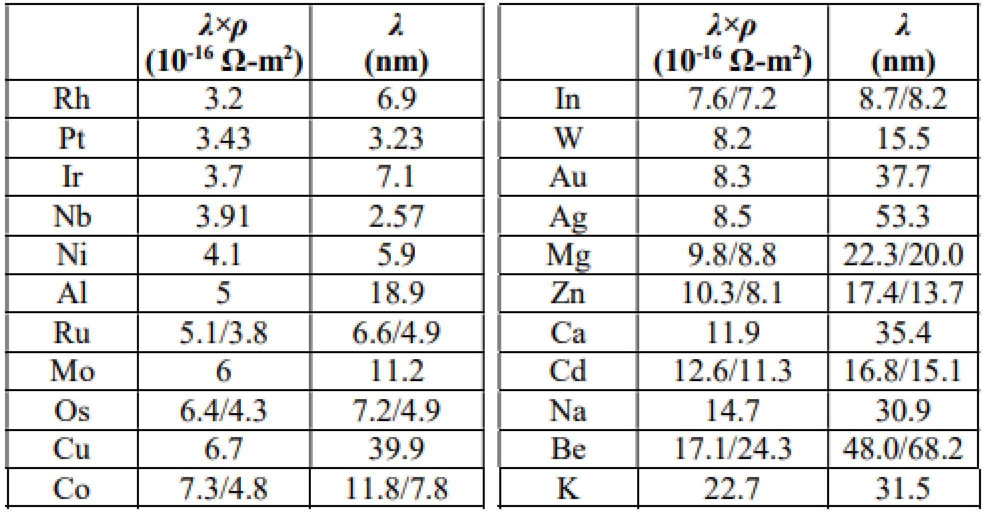
3 Insitu-liner Process

⬇

Bulk ALD Deposition

Eliminates the need for TiN liner ➡ **Improves WL resistance in thinner tier pitch structures**

D. Gall, "Metals for Low-Resistivity Santa Clara, CA, USA, 2018, pp. 157-159

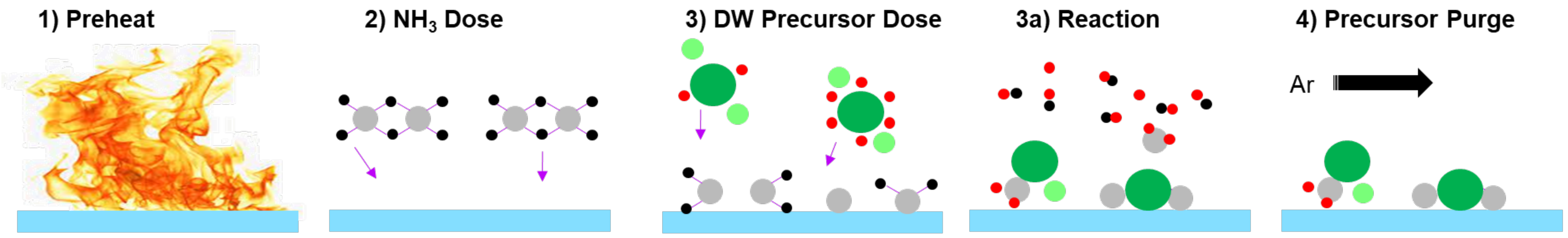


	$\lambda \times \rho$ (10^{-16} Ω-m^2)	λ (nm)		$\lambda \times \rho$ (10^{-16} Ω-m^2)	λ (nm)
Rh	3.2	6.9	In	7.6/7.2	8.7/8.2
Pt	3.43	3.23	W	8.2	15.5
Ir	3.7	7.1	Au	8.3	37.7
Nb	3.91	2.57	Ag	8.5	53.3
Ni	4.1	5.9	Mg	9.8/8.8	22.3/20.0
Al	5	18.9	Zn	10.3/8.1	17.4/13.7
Ru	5.1/3.8	6.6/4.9	Ca	11.9	35.4
Mo	6	11.2	Cd	12.6/11.3	16.8/15.1
Os	6.4/4.3	7.2/4.9	Na	14.7	30.9
Cu	6.7	39.9	Be	17.1/24.3	48.0/68.2
Co	7.3/4.8	11.8/7.8	K	22.7	31.5

NAND PROCESS | DW Deposition

A) Liner Deposition

🟩 Bulk DW
Liner
Oxide Substrate


1) Preheat

2) NH_3 Dose

3) DW Precursor Dose

3a) Reaction

4) Precursor Purge

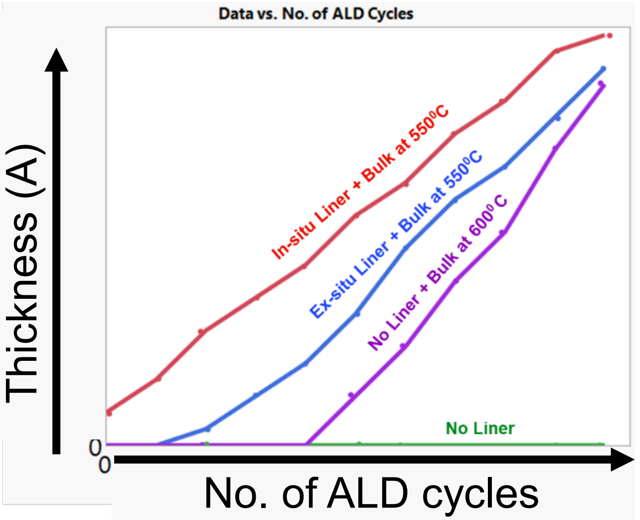
NAND PROCESS| DW Deposition Challenges

Nucleation Delay

Dielectric surfaces of growth cause sluggish nucleation and incomplete reactions.

Solution : DW Liner, High Temperature deposition

- Very High temperatures can cause substrate damage
- DW Liner is needed to optimize the trade off between high temperature and substrate damage



Fill issues

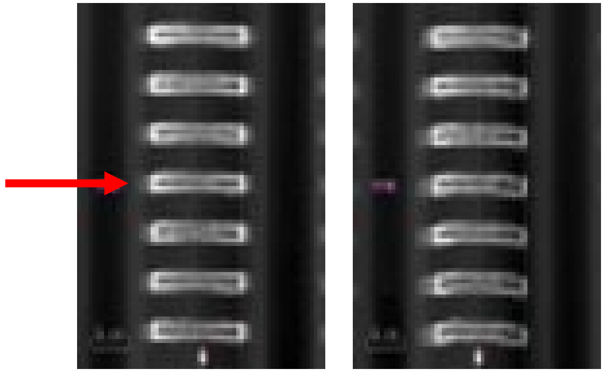
As two metallic films grow together, they experience surface attraction forces.

- Early pinch off

Inability of DW to fill in HAR, thinner tier pitch structures

- f (design dimensions, nucleation delay, process gaps)

Solution : Process and incoming structure optimization

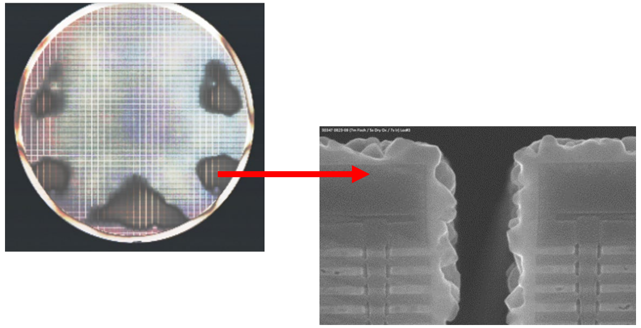


Hardware Stability

Particles concerns, premature throttle valve failures, solid precursor handling issues and unconverted rough DW films.

- Impact to productivity and HV enablement

Solutions: Continuous improvement in HW parts, HW stabilization through pre – deposition and process optimization.



NAND PROCESS| Optimization

To minimize defects, improve film quality, and enhance process yield

Pressure

Adsorption – Desorption dynamics

1. High pressure -Improves surface saturation for precursors but impacts diffusion

2.Low pressure – lowers surface coverage and improves diffusion

Concentration

Chemical reactions and Nucleation

1. Low concentration – smooth growth but slow dep rate

2. High Concentration - Rapid deposition, can case uncontrolled nucleation, hence voids

Temperature

Precursor decomposition rate and surface mobility

1. Raising temperature reduces the ΔG, but very high T may result in very rough morphology films, substrate damages and cell degradation

NAND PROCESS| Optimization

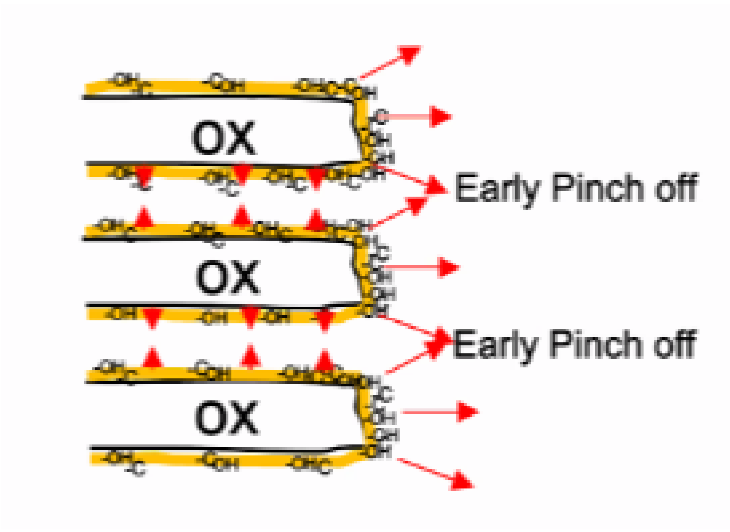
Role of impurities on nucleation of DW and fill in subsequent electrical behaviors

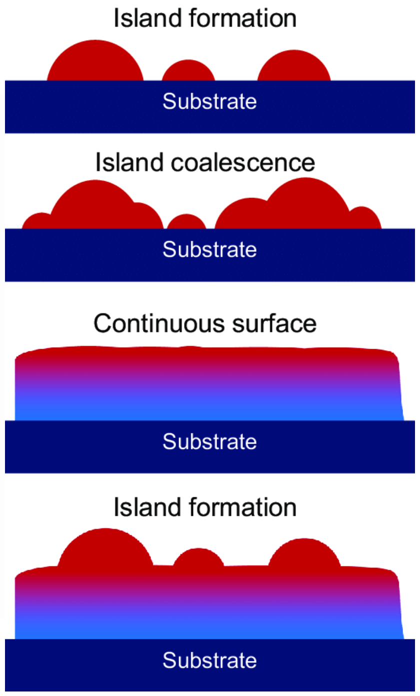
Surface contamination – Oxygen, carbon, halides either in bulk or interface

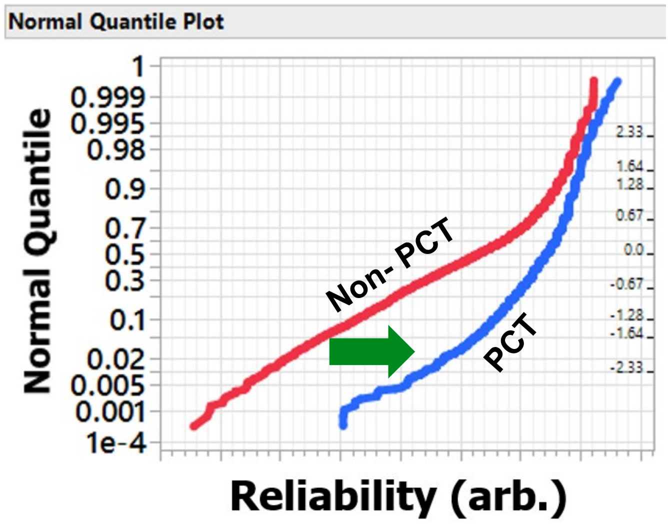
Non uniform nucleation or nucleation delay at high concentrations → grain size and grain boundary density

Variations in threshold voltage and charge leakage due to interface damages

Mitigated by surface treatments & tuning purge/temperature cycles in DW deposition







Yang, Fan & Wang, Chao & Bai, Haiyang & Wang, Weihua & Liu, Yanhui. (2021) Communications Materials. 2. 75. 10.1038/s43246-021-00180-9.

*Pressure, Concentration, Temperature

CONCLUSIONS

1. XYZ scaling poses unique metallization challenges – Need material switch from W
2. Along with several optimizations, PCT tuning plays a key role is improving the WL fill and resistance
3. Addressing impurities in WL or interface is key to achieve consistent electrical behaviors
4. Process optimizations, integration changes to establish-reestablish the material property change interactions

ACKNOWLEDGEMENTS

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2. **Micron Team:** Co-authors and collaborators Swapnil, Haoyu, Rita, Allen, Roland, Quek, Ramanathan, Arvind, Timothy, Bhavesh, Calvin, Krishnan, Mark Kiehlbauch

3. **Shubham Kapoor** – silent supporter and the one who dealt with my DW Mood the most.

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