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Heterogeneous Integration: Al Inspired. Systems Accelerated

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The Al Era is Changing the Landscape of Technology and Product Development



Structural Shifts In Customer Needs

AI / HPC Has Surpassed Mobile Revenue



Systems of Chips Chiplets Surpass Monolithic by 2028

ource: IHS, SemiAnalys



Source: Gartne

Vertical Integration ≤5nm Wafer TAM: 4% in 2024 to 12% in 2030



Challenge: Mismatch In Scaling



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HW FLOPS (required): ~60,000x / 20yrs

Up to 30x GAP! = brute force (high cost, power) Needed to scale AI

=Inefficient systems

2032 2033

The Path Forward



Systematic Path to Exponential Improvement

System Revolution

System Evolution

System Technology Co-Optimization Reduced precision numbers New memories & network topologies Model efficiency

Evolve standards e.g. serial HBM, AIC Moore's law + packaging

Hardware optimized for software Memory, compute, networking in harmony

Time

Heterogeneous Integration & Systems Foundry



Systems Foundry For The AI Era



Angstrom Era Silicon Innovations

RibbonFET Transistors

PowerVia Interconnects



Gate All Around



Innovation In Transistors

Better electrostatics compared to FinFETs Optimized ribbon architecture for best Perf/W & Vmin

Traditional



Innovation in Interconnect

Improved density & cell utilization Reduced resistive power delivery droop

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PowerVia



Advanced Packaging, Assembly and Test Differentiation In Action



Comprehensive technology, design, and manufacturing to enable System-Technology Co-Optimization (STCO)

Systems Foundry Approach to Design Enablement

Design enabling from concept to tapeout ensuring successful system-of-chips product development





Enhancing Integration and Power Efficiency



Power Efficiency





Sustainable Systems Innovations for Al's Next Frontier

Turning a Corner



Truly Differentiated





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Results

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